

Sequential Machine Fundamentals

5-20. Using timing diagrams analyze the operation of:
(a) The clocked RS Flip-Flop shown in Figure 5-22.
(b) The clocked D-Latch shown in Figure 5-23.

5-21. Discuss why the avoidance of the indeterminability of a binary cell becomes increasingly important where clocked RS Flip-Flops are being used.

5-22. By making a simple transformation, convert the RS Flip-Flop shown in Figure 5-22 to support the following schematic symbol (Figure P5-4).

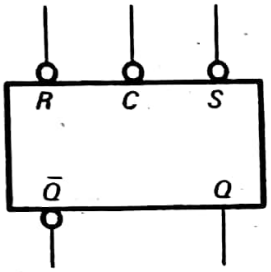


Fig. P5-4.

5-23. Using a timing diagram approach, analyze the T Flip-Flop shown in Figure 5-24. Include propagation delay in your analysis, illustrating the undesirable mode of operation (oscillation or hang) discussed in Section 5-15.

5-24. Using the steps set forth in Section 5-17:
(a) Design a NAND cell centered LM Flip-Flop specified by the following characteristic table and schematic symbol (Figure P5-5).

L	*M*	*Qn*	*Qn*+1
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

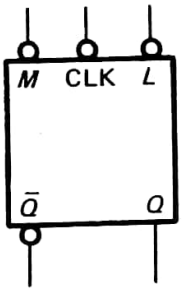


Fig. P5-5.

(b) Define the excitation table for the LM Flip-Flop.

5-25. Using the steps set forth in Section 5-17:
(a) Define the characteristic table.
(b) Design a NAND cell-centered Flip-Flop.
(c) Define the excitation table for a SET dominant clocked SR Flip-Flop. This Flip-Flop is to always leave the basic cell in a SET condition if *S* and *R* are asserted together. Design in asynchronous SET and RESET functions.

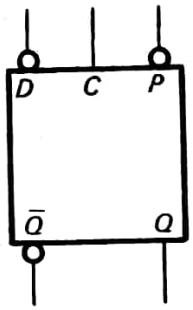
5-26. Repeat the steps specified in Problem 5-25 for the following design problem: Design a RESET dominant clocked RS Flip-Flop. This Flip-Flop is to always leave the basic cell in a RESET condition if *S* and *R* are ASSERTED together. Design in asynchronous SET and RESET functions.

5-27. Repeat the steps specified in Problem 5-25 for the following design problem: Design a RS Flip-Flop that will leave the basic cell unchanged if the *S* and *R* are ASSERTED together.

5-28. Design a Flip-Flop specified by the following characteristic table. Check your circuit with Figure 5-25(b).

	J	*K*	*Qn*	*Qn*+1
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

5-29. Using all the information available, design a NOR cell centered POOPS-DINK (*P*,*D*) Flip-Flop that operates as specified by the following table and schematic symbol (Figure P5-6):

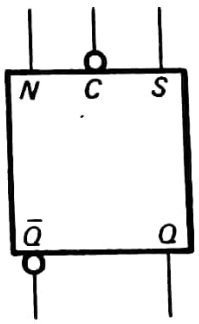


P	D	*Operation*
0	0	Changes state with clock only if $Q=1$
0	1	Changes state with clock only if $Q=1$
1	0	Always sets the Flip-Flop with clock
1	1	Changes state with clock.

Fig. P5-6.

(a) Show general model of your Flip-Flop.
(b) Define the characteristic table.
(c) Define the excitation table.
(d) Show completely documented schematic diagram.

5-30. Repeat Problem 5-29 for the SN Flip-Flop that is specified by the following table and schematic symbol (use NAND cell) (see Figure P5-7).



S	*N*	*Operation*
0	0	Changes state with clock only if $Q=0$
0	1	Changes state with clock only if $Q=1$
1	0	Always sets with clock
1	1	Remains unchanged

Fig. P5-7.

5-31. Is it possible to design a T Flip-Flop that triggers on the rising-edge of the clock and within reasonable limits avoid the oscillation or hang problems associated with T Flip-Flops? Outline your method of attack for solving the problem.

5-32. Using the method outlined in Section 5-18, carry out the following conversions.
(a) Convert a D-Latch to a JK.
(b) Convert a JK Flip-Flop to a D-Latch.
(c) Convert a JK Flip-Flop to a T.
(d) Convert a T Flip-Flop to a JK.

5-33. Using the method outlined in Section 5-18, carry out the following conversions.
(a) Convert a D Flip-Flop to the PD Flip-Flop specified in Problem 5-29.
(b) Convert a JK Flip-Flop to the SN Flip-Flop specified in Problem 5-30.

5-34. In your own words discuss the "hows" and "whens" the 1's and 0's catching problem arises when using a MASTER/SLAVE Flip-Flop. How does the asynchronous input create a problem?

5-35. Design, using the methods outlined, a D MASTER/SLAVE Flip-Flop.

5-36. In your own words discuss the three types of JK Flip-Flops triggering discussed in Section 5-19. Draw comparisons between the three and list what you see as advantages and disadvantages of each.

5-37. Draw a timing diagram and illustrate your understanding of SETUP and HOLDING time. Give a qualitative description of each and how these specifications relate to the hardware of the Flip-Flop.

5-38. In your own words discuss clock skew. Discuss why clock skew can create data transmission problems.

5-39. Consider you are far off in Futz-a-too and you have burned out your last J-K falling-edge trigger Flip-Flop which was used as a T Flip-Flop with T ASSERTED LOW. But all is not lost—you have one rising-edge triggered D Flip-Flop, and the following gates (not packages) on your board: one INVERTER, one two-input OR gate, and two two-input NAND gates.
(a) Using these devices *design* (show all design work) a circuit which will replace your burned out T Flip-Flop. (i) Draw your conversion model. (ii) Draw your circuit.
(b) You are given the following propagation delay parameters:

Inverter—10 nsec
All two-input gates—20 nsec
D Flip-Flop
—set up time = 20 nsec
—hold time = 5 nsec

What is the set up and hold time for your new Flip-Flop?